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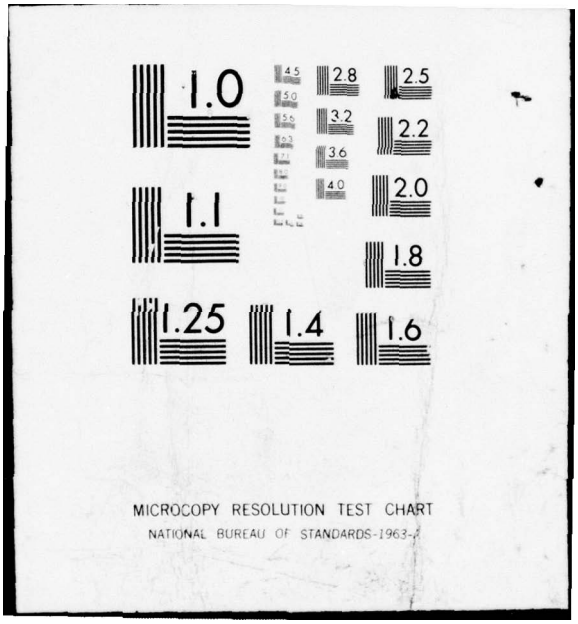
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TRACKING SERVOBRIDGE DETECTOR
FIRST QUARTERLY PROGRESS REPORT

for period

21 June 1973 through 30 September 1973

CONTRACT NO. DAAB05-73-C-0609

Industrial Management Division
Procurement and Production Directorate
U. S. Army Electronics Command

GENERAL RADIO COMPANY
Concord, Massachusetts 01742

This project has been accomplished as part of the U. S. Army Advance Production Engineering Program, which has as its objective the timely establishment of manufacturing processes, techniques, or equipment to ensure the efficient production of current or future defense programs.

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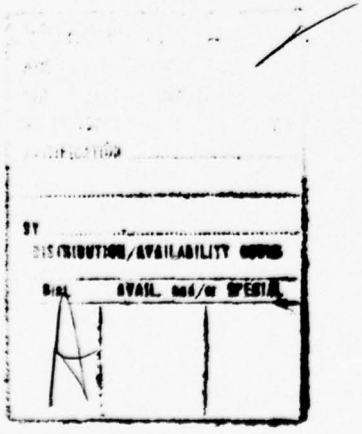
TRACKING SERVOBRIDGE DETECTOR
FIRST QUARTERLY PROGRESS REPORT
for period
21 June 1973 through 30 September 1973

The object of this study is to establish production engineering measures to be undertaken for the parts, materials and processes used in fabricating tracking servobridge detectors; and to establish the producibility of that item by mass production techniques and with mass production facilities; establish a quality control system; and take such actions as necessary to reduce the time required for delivery of the subject items that will be required in large quantity production for current planning and in the event of an emergency.

Contract No. DAAB05-73-C-0609

Prepared by:

H. P. Stratemeyer



Section 1

ABSTRACT

1.0 General

This report summarizes the work done to date on the X10 Frequency Multiplier and Broadband Power Amplifier sections of the Tracking Servo Bridge Detector. Preliminary design decisions and general concepts for other component system sections are also described.

1.1 X10 Frequency Multiplier

Circuit design has been completed and a breadboard built, evaluated, and found to perform within specifications. The design particulars are described with full circuit diagrams. As required, the multiplier generates an rf output of 45 to 220 MHz from a reference input signal of 1/10 the output. The power level of the generated signal is +10 dBm into 50 ohms with all harmonics more than 25 dB down. Automatic gain control is included for distortion control. A digital phase-frequency detector is employed to ensure that phase-lock occurs only at 10 times the reference input frequency. This design also permits the unlock alarm system to signal a wide variety of system failures.

1.2 Broadband Power Amplifier

An early intention to buy a commercially available amplifier gave way to a decision to design for specific system requirements. The resulting amplifier design has been proven in breadboard form to more than meet applicable specifications and display excellent efficiency as well. The make-buy considerations are discussed in detail as are the design factors

that resulted in outstanding performance. Power output and distortion of the amplifier as functions of frequency are plotted graphically from actual measurements and are shown to comfortably meet requirements. The Return Loss (VSWR) performance is outside specifications at high frequencies and the text discusses reasons to expect that the etched-circuit form of the amplifier will not display this deviation.

1.3 Other System Components

Three additional parts of the Tracking Servo Bridge Detector have received attention and stand at various degrees of completion. Exact status is described for the Reference IF and Phase Shifter, Detectors, and Power Supplies.

Section 2

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Section 3

PURPOSE

This contract is to establish production processes for the manufacturer of the parts, materials and assemblies used to fabricate Tracking Servobridge Detectors, meeting the requirements of Specification No. MIL-D-55361 dated 27 January 1972 with Amendment 1 of Contract No. DAAB05-73-C-0609. Under production engineering measures, the contractor will establish or improve the producibility of the subject Detectors by mass production techniques and with mass production facilities; establish a quality control system, where nonexistent, and improve existing quality control systems; and take such actions necessary to reduce the time required for delivery of the contracted item that will be required in large quantity production for current planning and in the event of an emergency. The objective is to support the establishment of a production capability for the purpose of meeting estimated military needs for a period of two years after completion of the contract, and to establish a base and plans which may be used to meet expanded requirements.

The Tracking Servo Bridge Detector is used in conjunction with standard RF bridges for the purpose of measuring quartz crystal parameters with high accuracy. The basic system arrangement is shown in Fig. 3.1. The Tracking Servo Bridge Detector functions as a very sensitive detector for the bridge unbalance signal, permitting crystal measurements at power levels well below one microwatt. Synchronous detectors provide independent reactive and resistive unbalance detection. A complete control loop may be used to "lock" the synthesizers frequency to the crystal under test, automatically maintaining bridge balance.

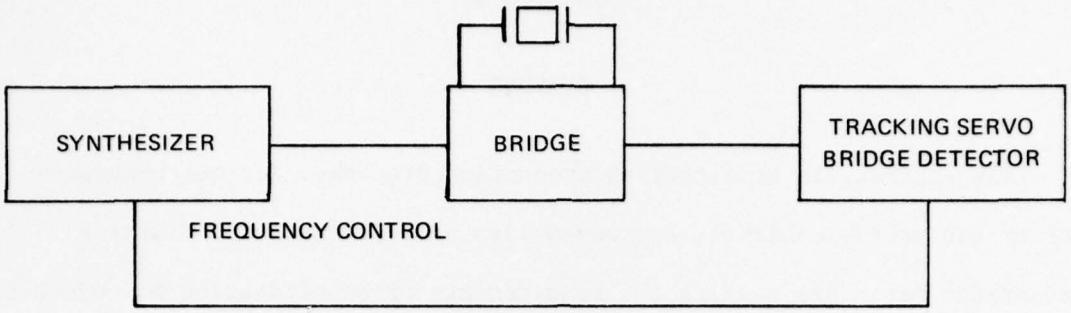


Figure 3.1 Basic System Arrangement

The frequency range covered is .8 - 220 MHz. Provisions are made for oscilloscope display, for swept frequency operation. This permits inspection for spurious modes and assists in the initial set-up for the desired precision measurement. Other features are a broadband power amplifier with attenuator (to amplify the synthesizers signal) and a X10 frequency-multiplier to extend synthesizers of limited frequency range. The objective in the design concept was to provide all needed auxiliary functions for the crystal measurement with a bridge, other than the signal source (synthesizer), frequency measuring equipment, and oscilloscope. The accuracy of the measurements is limited only by the RF-bridge used.

4.0 NARRATIVE AND DATA

4.1 X10 Frequency Multiplier

4.1.1 Introduction

The basic Tracking Servo Bridge Detector requires two RF drive signals, one at the measurement frequency (0.8-220 MHz) and the second offset from it by the IF frequency (80 kHz). Provision is made for the inclusion of a special SSB generator to produce the offset frequency, in which circumstance only a single RF source is required. The requirements for this RF source are further eased by the inclusion of a X10 Frequency Multiplier which reduces to 22 MHz the upper frequency needed.

The specifications for the X10 Frequency Multiplier call for an input of 4.5 - 22 MHz at a power level of +10 dBm and an output of 45-220 MHz at the same power level, with all harmonics at least 25 dB down. The unit can have up to five overlapping bands and must not degrade the signal-to-phase-noise ratio of a high-purity synthesizer source by more than 6 dB in excess of that caused by X10 frequency multiplication alone.

These requirements can best be met by the phase-locked-oscillator multiplier (PLOM) system employed in this Tracking Servo Bridge Detector design and shown in the block diagram Figure 4.1.1.1 and the schematic diagram of Figure 4.1.1.2.

A voltage-controlled oscillator at the output frequency is phase-locked to 10 times the input frequency by means of a decade divider within a phase-lock loop. The system blocks are described in the following sections of this report.

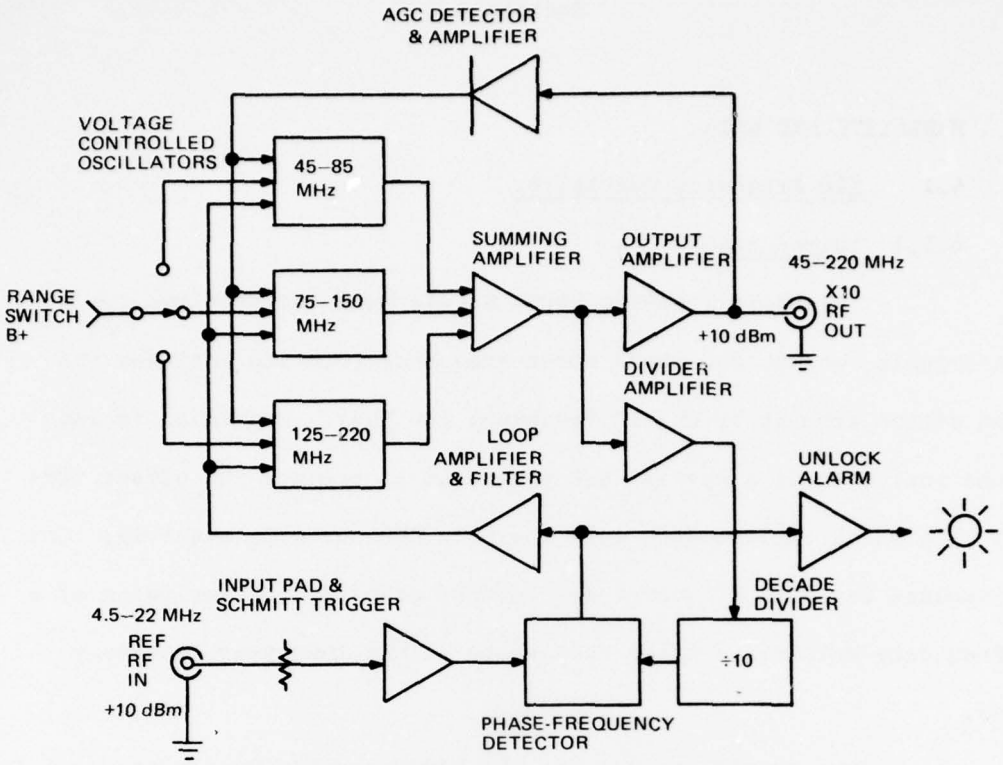
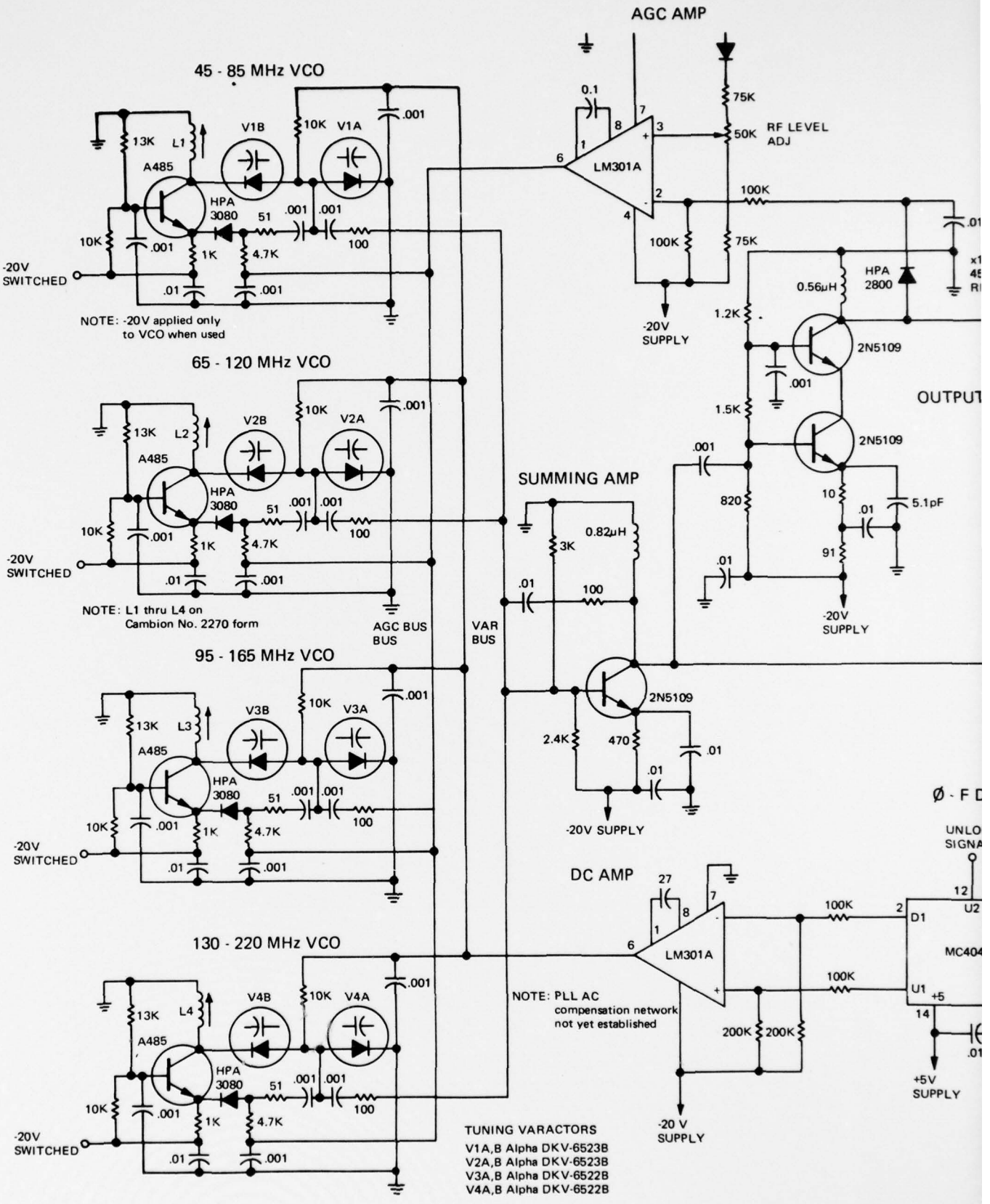


Figure 4.1.1.1. Block Diagram of X10 Frequenc / Multiplier.

4.1.2 Voltage Controlled Oscillators

The heart of the X10 Frequency Multiplier is a set of three voltage-controlled oscillators (VCO's) each having a tuning ratio of nearly 2:1. The three ranges are 45-85 MHz, 75-140 MHz, and 125-220 MHz which cover the overall 45-220 MHz range with overlaps of 10 and 15 MHz.

Figure 4.1.2 is the VCO circuit diagram; the oscillator circuit is identical for each of the three ranges except for the tank coil and tuning varactors. It is a grounded-base amplifier with positive feedback from collector to emitter. The impedance step down in the feedback path, which is a necessary condition for oscillation, is accomplished by tapping off at the junction of the two series-connected tuning varactors. Alternate methods, such as link coupling, an inductive tap, or a separate capacitive divider, are less satisfactory. They have the disadvantages of a more compli-


AGC AMP
45 - 85 MHz VCO
65 - 120 MHz VCO
95 - 165 MHz VCO
130 - 220 MHz VCO
SUMMING AMP
DC AMP
LM301A
RF LEVEL ADJ
50K
75K
100K
0.1
.001
.01
.1
13K
10K
1K
4.7K
51
100
1.2K
1.5K
820
3K
2.4K
470
91
10
5.1pF
0.56µH
0.82µH
HPA 2800
HPA 3080
A485
2N5109
V1A
V1B
V2A
V2B
V3A
V3B
V4A
V4B
L1
L2
L3
L4
-20V SWITCHED
-20V SUPPLY
+5V SUPPLY
AGC BUS
VAR BUS
OUTPUT
NOTE: -20V applied only to VCO when used
NOTE: L1 thru L4 on Cambion No. 2270 form
NOTE: PLL AC compensation network not yet established
TUNING VARACTORS
V1A,B Alpha DKV-6523B
V2A,B Alpha DKV-6523B
V3A,B Alpha DKV-6522B
V4A,B Alpha DKV-6522B

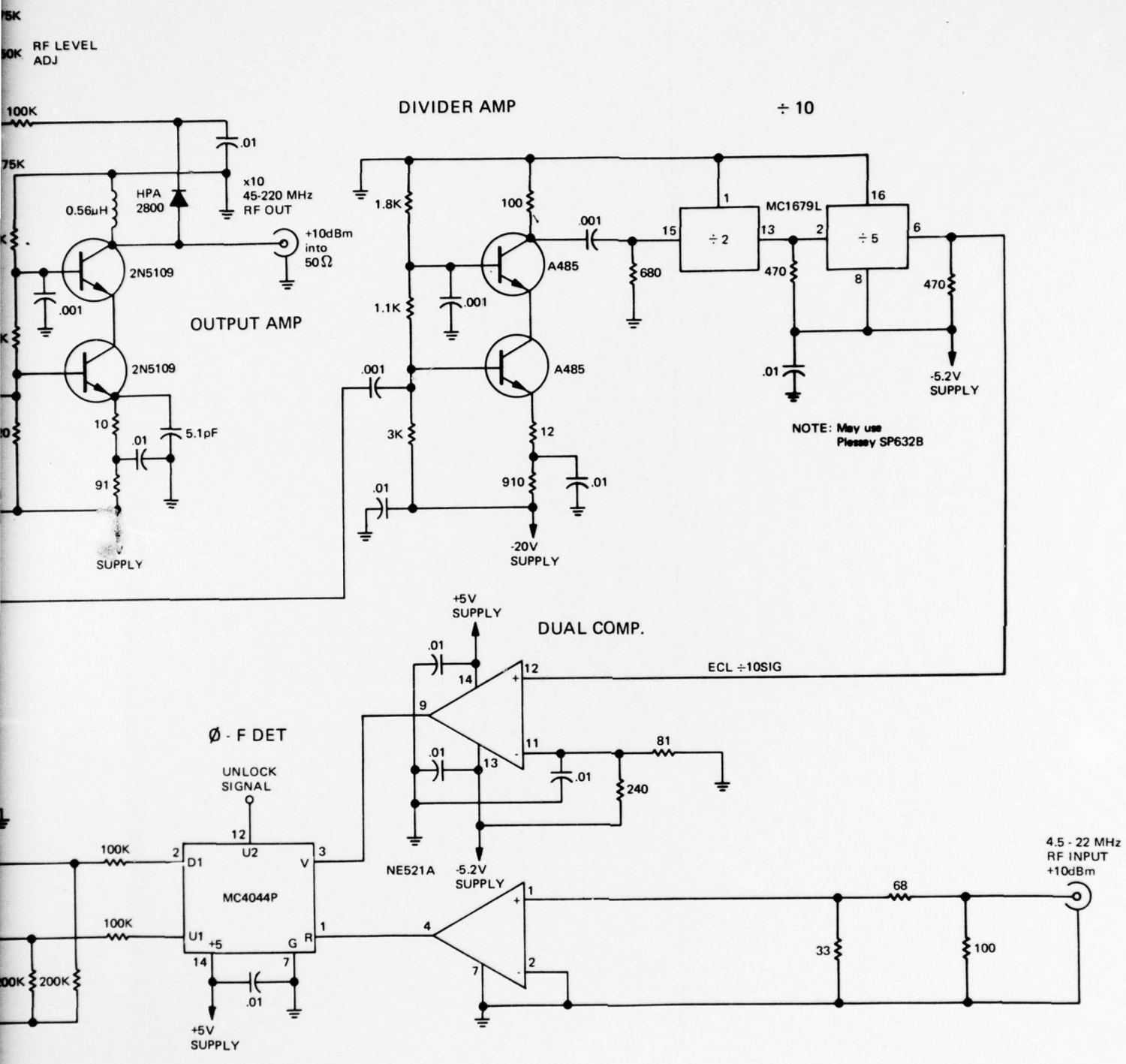


Figure 4.1.1.2 Schematic Diagram of X10 Frequency Multiplier

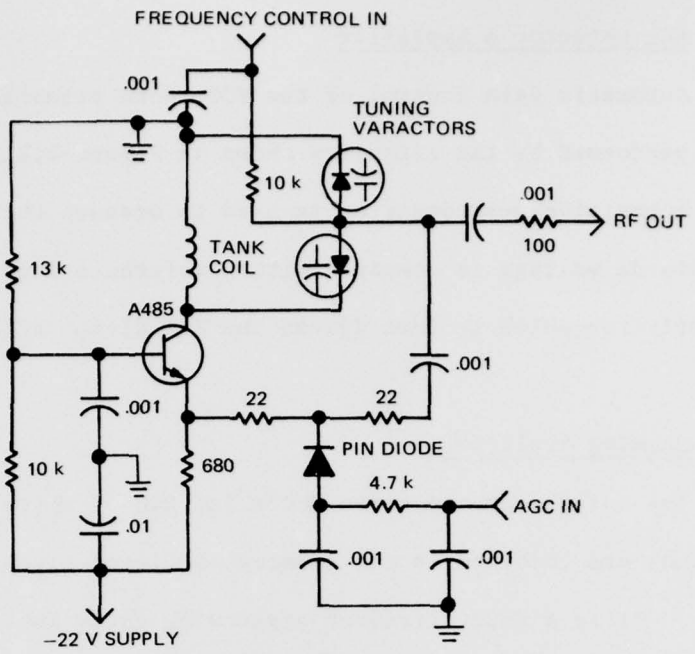


Figure 4.1.2. Voltage-Controlled Oscillator.

cated tank coil and troublesome leakage reactance problems, or of additional shunt capacitance which restricts the tuning range.

If the harmonic distortion of the oscillator output signal can be kept to about 30 dB below the fundamental level, low pass filters will not be required. A complex filter configuration would be necessary to provide significant second harmonic attenuation over a frequency range of nearly 2:1. Low harmonic levels are obtained directly by the use of an automatic-gain-control (AGC) loop which senses the output from the X10 multiplier and varies the oscillator loop gain to prevent saturation. A PIN diode is used as a variable rf attenuator in the oscillator feedback path to accomplish this function. The PIN diode is polarized as shown to provide isolation between the AGC bus and all "off" VCO's.

4.1.3 AGC Detector & Amplifier

Automatic gain control of the VCO, done primarily to reduce distortion is performed by the circuitry shown in Figure 4.1.3.

A positive-peak detector is used to measure the +10 dBm output level. This dc voltage is compared with a reference level by an operational amplifier which in turn drives the PIN diode variable attenuator in the VCO.

4.1.4 Summing Amplifier

The outputs of the three VCO's (no two of which can be active at the same time) are combined in the summing amplifier circuit shown in Figure 4.1.4. It is a shunt feedback stage with three input resistors which operates in the same manner as a summing operational amplifier. The stage is designed to have the required frequency response (45-220 MHz) and harmonic distortion ($>$ 30 dB down).

4.1.5 Output Amplifier

The required +10 dBm output from the X10 multiplier unit is produced by the cascode amplifier stage shown in Figure 4.1.5. Each of the two 2N5109 transistors has a power dissipation of 220 mW, well within it's 75°C ambient rating of 700 mW. The summing amplifier and cascode output stage have a combined gain of 18 dB when driven from a 50Ω source matched with a 50Ω input resistor. The gain is flat to within $\pm$1 dB over the 45-220 MHz band and all harmonics are down 35 dB or more while producing +10 dBm into a 50Ω load. In the actual instrument, this output drives a power amplifier which produces the drive power for the rf bridge.

4.1.6 Divider Amplifier

The summing amplifier also drives a second cascode amplifier which provides the input for an ECL decade divider. This amplifier has sufficient isolation to keep spurious components from the digital logic down by about 60 dB in the VCO output. Details are shown in Figure 4.1.6.

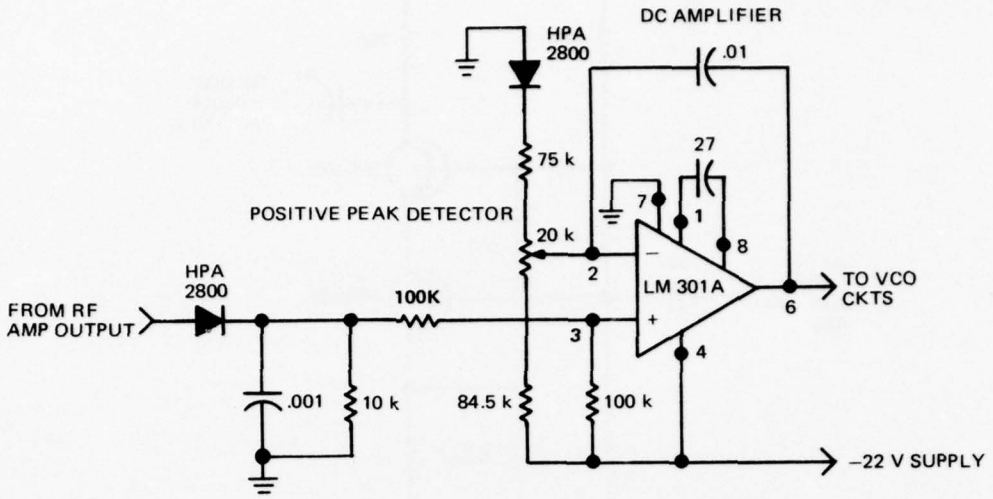


Figure 4.1.3. AGC Detector & Amplifier.

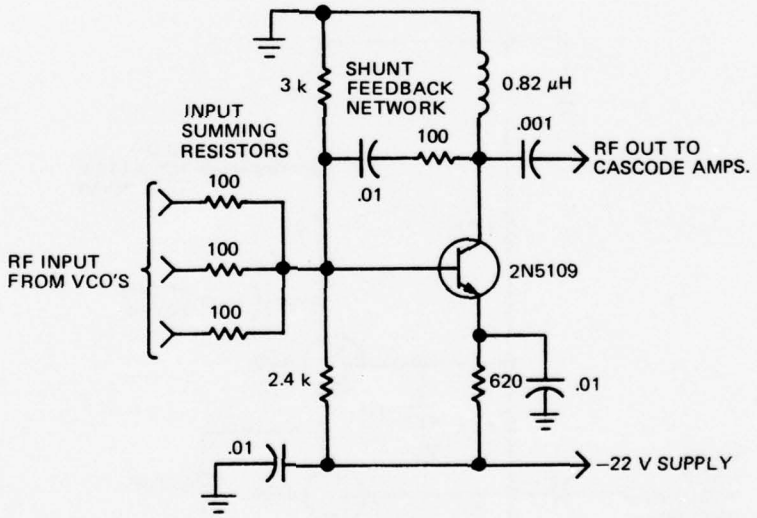


Figure 4.1.4. Summing Amplifier.

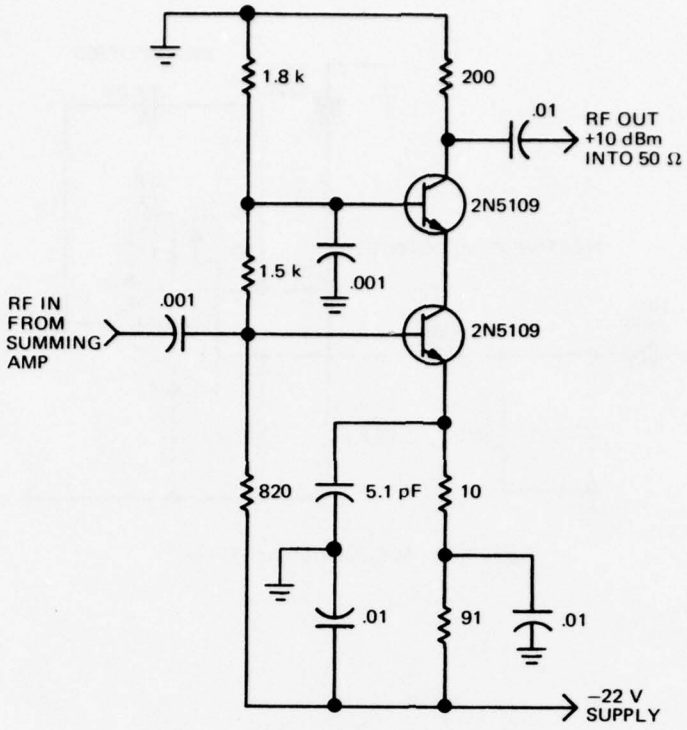


Figure 4.1.5. Output Amplifier.

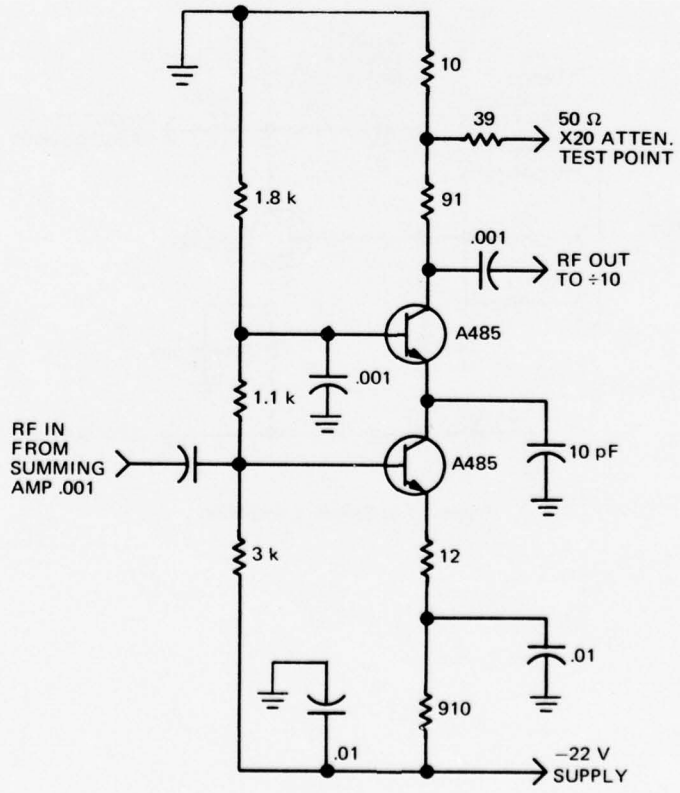


Figure 4.1.6. Divider Amplifier.

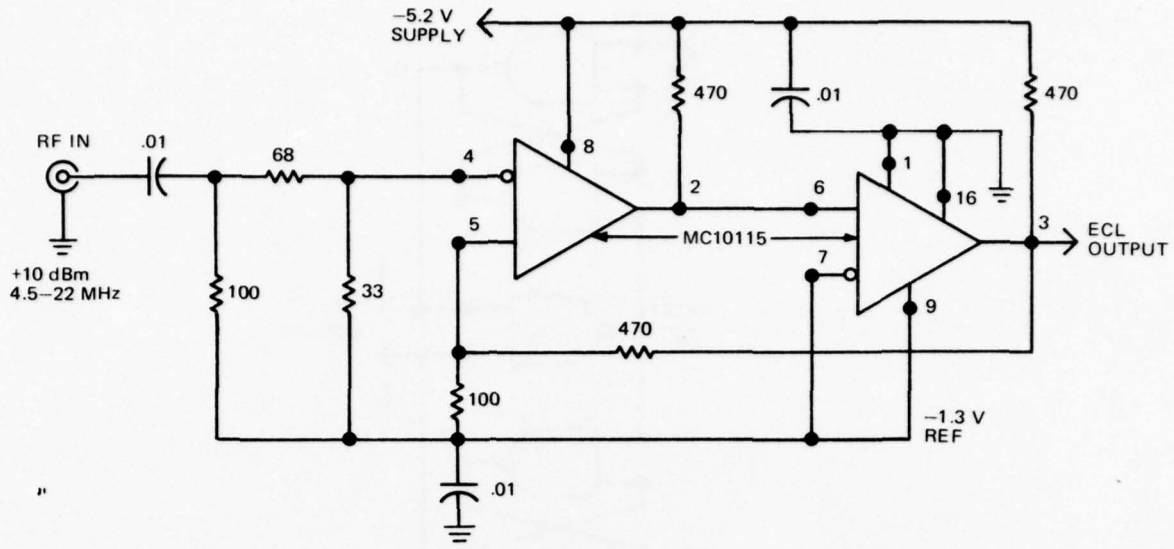


Figure 4.1.8. Input Schmitt Trigger.

4.1.7 Decade Divider

This is a straightforward application of an ECL decade divider. The Plessey SP632B device used is specified for sinusoidal input signals from 40 to 400 MHz.

4.1.8 Input Schmitt Trigger

The rf reference input signal (which is to be multiplied in frequency by a factor of ten) is applied to the circuit shown in Figure 4.1.8. It consists of a 10-dB pad with 50Ω input impedance and two ECL differential amplifiers connected in series, with positive feedback. This Schmitt trigger circuit is used to convert the +10 dBm sinusoidal input into a signal having an ECL waveform.

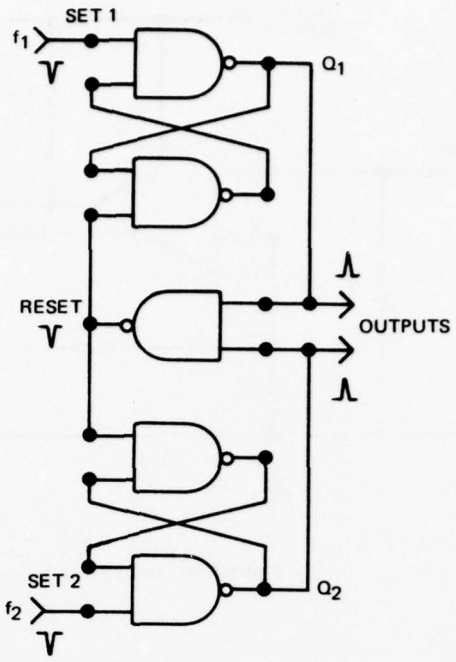


Figure 4.1.9.1. Phase-Frequency Detector.

4.1.9 Phase-Frequency Detector

It is highly desirable to augment the usual phase-detector function with a frequency-difference indication in a multiplier system of this type. This not only insures that the phase-lock loop will "capture" but also insures that lock will occur only at a VCO frequency ten times that of the reference input.

The basic phase-frequency detector logic used is shown in Figure 4.1.9.1. It consists of two set-reset latches (each implemented with two 2-input positive NAND gates) and another gate which is used as a reset generator. The operation of the circuit is as follows: The first input pulse to arrive sets its corresponding latch. The circuit will remain in this state until a pulse arrives at the other input (whether or not additional pulses arrive at the first input). The pulse at the other input first sets that latch and then the reset gate immediately resets both latches. Thus the circuit will produce the following outputs:

$f_1 > f_2$ The Q_1 output will be a variable duty ratio pulse train, varying from approximately 0 to 100% at the rate $\Delta f = f_1 - f_2$. The Q_2 output will be low except for the duration of the narrow input pulse.

$f_2 > f_1$ The Q_1 and Q_2 outputs will be the reverse of that described above.

$f_1 = f_2$ One of the two outputs will be low except for the duration of the narrow input pulse.
The other output will be a certain fixed duty ratio which is dependent on the phase relation of the two input signals.

In use in a phase-lock loop with high dc gain, this phase detector will operate at a nominal 0° phase relation. Both outputs will be low except for identical positive pulses during the duration of the (coincident) input pulses. The output, which is taken differentially, is the nearly-zero signal determined by the static error coefficient set by the dc loop gain. Since both outputs are identical it becomes immaterial from which direction the loop approached lock. But before lock, when $f_1 \neq f_2$, an error signal is produced which forces the loop toward the condition $f_1 = f_2$ and $\phi_1 = \phi_2$.

The phase-frequency detector also contains a pulse generator for each input as shown in Figure 4.1.9.2. A D-Type flip-flop is triggered by the positive-going transition of the input signal, causing the Q output to go positive. This output, delayed by passing through a gate, is used to reset the flip-flop. The circuit thus generates a positive pulse which has a duration equal to the propogation delay of the gate plus that of the flip-flop reset input.

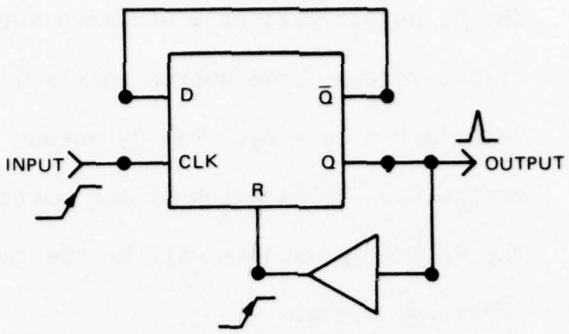


Figure 4.1.9.2. Pulse Generator.

4.1.10 Unlock Alarm

The phase-frequency detector produces coincident output pulses only under locked conditions. This is the operating principle of the unlock-alarm circuit shown in Figure 4.1.10.

The coincidence of the detector pulses is sensed by the exclusive-or logic function which has an output that is high when the loop is locked and a variable duty ratio pulse train when the loop is unlocked. The resulting change in dc voltage is detected by a comparator which drives the unlock-alarm light. The unlock alarm will warn of any of the following conditions:

1. No reference signal.
2. No oscillator signal.
3. Reference signal outside lock range of oscillator.
4. AC on lock loop for any reason.
5. Failure of the Summing Amplifier, Divider Amplifier, Decade Divider, Pulse Generators, or Input Schmitt Trigger.
6. Loss of -5.2 V supply.
7. Most failures of Phase-Frequency Detector.

Loss of the -22 V supply, while not indicated by the alarm, will

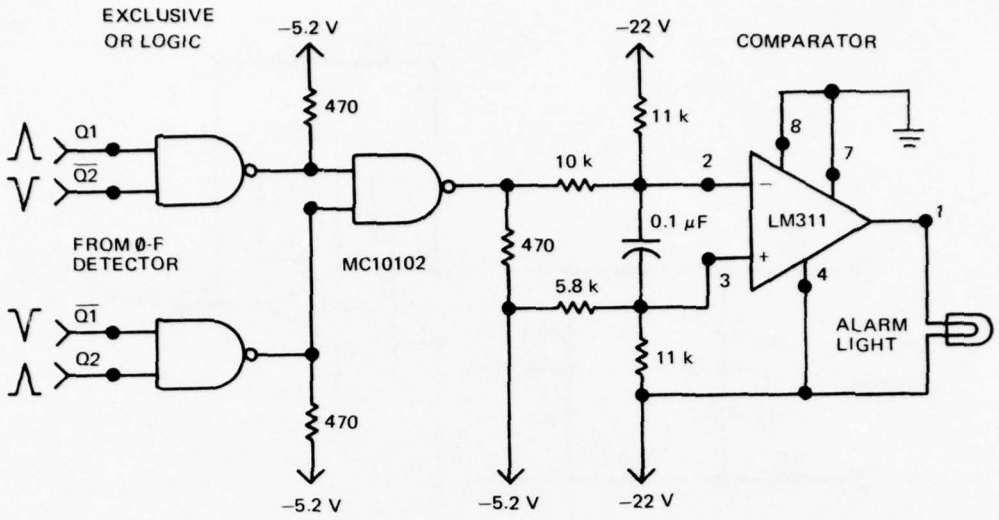


Figure 4.1.10. Unlock Alarm.

result in no output from the multiplier, thus no wrong output. The alarm circuit itself can be checked by simply removing the reference signal and observing that the alarm light comes on.

4.1.11 Phase-Lock Loop DC Amplifier & Compensation Network

The phase-frequency detector produces two output signals which are used as the inputs of a differential amplifier that closes the overall phase-lock loop. Several passive networks ahead of and associated with the operational amplifier, shown in Figure 4.1.11.1, serve to shape the frequency response of the loop and thus ensure a stable servo-system.

Detailed analysis of phase-lock loop behavior has appeared in the technical literature numerous times and will not be repeated here. The basic open-loop response G, in the absence of any filters or other low pass breaks, is given by:

$$G = \frac{\omega_c}{s}$$

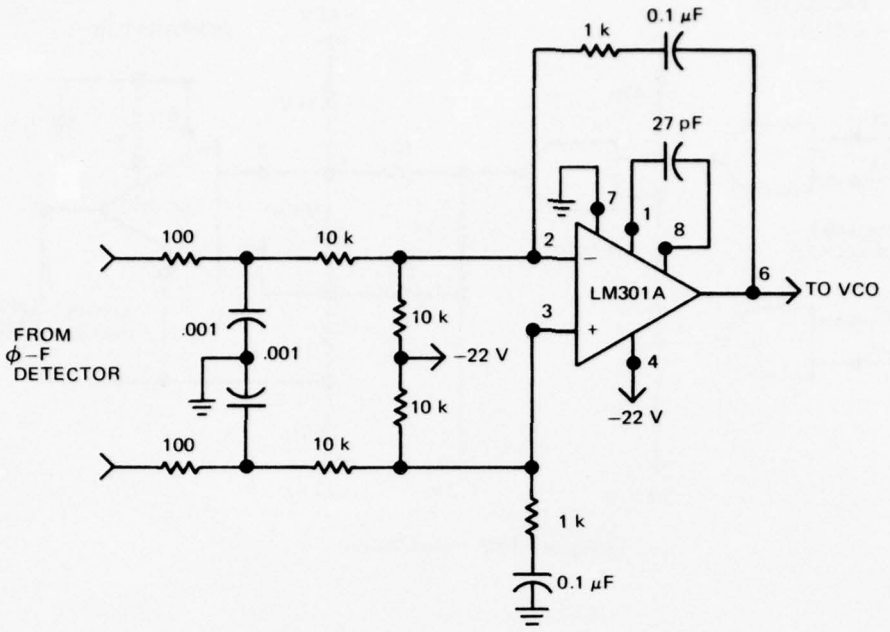


Figure 4.1.11.1. DC Amplifier & Loop Filter.

where $\omega_c = K_\phi K_a K_v$ rad/sec

and K_ϕ = phase detector sensitivity in volts/rad

K_a = amplifier gain in volts/volt

K_v = VOC tuning sensitivity in rad/sec per volt

The open-loop response is that of an ideal integrator, the result of the VCO block. Phase, the loop variable under consideration, is the integral of the VCO frequency. This response is shown in Figure 4.1.11.2. It is obvious that if any additional low-pass breaks exist near or below the frequency ω_c, the closed loop will be unstable.

It is often possible to use this natural rolloff characteristic by simply insuring that all other breaks are sufficiently higher than ω_c. This would result in the greatest possible loop bandwidth, a desirable condition for a frequency multiplier which must contribute the least possible phase noise to a stable reference signal.

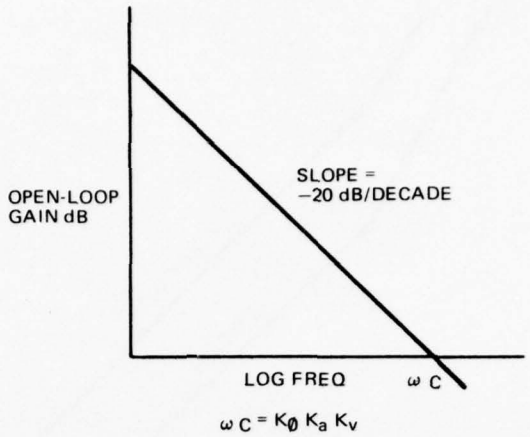


Figure 4.1.11.2. Basic PLL Open-Loop Response.

Unfortunately, such a simple approach is not practical in this instance. The value of $f_c = \omega_c/2\pi$ varies from between 0.5 and 2 MHz, and avoiding additional low-pass breaks to about 5 MHz is both impractical and undesirable.

The loop is therefore stabilized by means of a compensation network which rolls off the gain more rapidly in the region below about 2 kHz and then returns to a -6 dB/octave rolloff in the region where the open-loop gain becomes unity, now reduced to about 100 kHz. This shaping is done by the series RC feedback networks in conjunction with the source impedance. Additional networks provide high frequency filtering and dc translation.

The resulting open-loop response of the overall phase-lock loop is shown in Figure 4.1.11.3. Curves are shown for both minimum and maximum gain, a function of rf frequency and of the VCO in use. Although potentially unstable for conditions of both low and high gain, the system actually has a large margin in either direction. The loop provides at least 40 dB of negative feedback for VCO phase noise at sideband frequencies of 1 kHz and below.

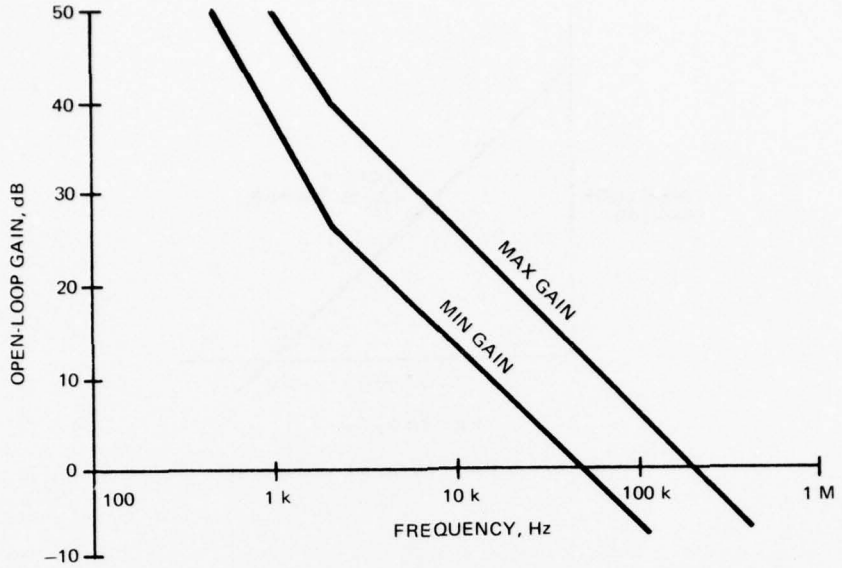


Figure 4.1.11.3. Actual PLL Open-Loop Response.

4.2 Broadband Power Amplifier

4.2.1 General

A broadband power amplifier (0.8-220 MHz) is required which exhibits low distortion and an output of at least +29 dBm from 0.8 to 20 MHz and at least +24 dBm from 20 to 220 MHz. It was originally planned to purchase a commercial power amplifier for use in the Servo Bridge Detector, but careful evaluation of available units showed none to be suitable. Most units are either too large or too expensive; some require forced air cooling, considered undesirable because of shielding problems. DC power requirements are usually between 20 and 30W for 1W rf output. Harmonic distortion is also a problem, most units being rated at between -16 dB and -26 dB. After considerable effort to find a suitable unit, it was decided to develop a special purpose amplifier. The unit developed meets the electrical requirements, is small (5 x 2-1/2 x 1-1/8 inches), and needs no forced air. The DC input is less than 10W and heat is dissipated by conduction through the case.

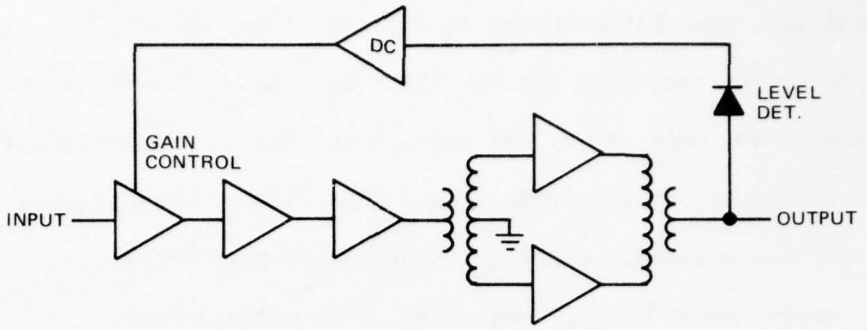


Figure 4.2.1. Power Amplifier.

The basic circuit is shown in Figure 4.2.1. The output stage is a push-pull transformer-coupled circuit. The lower level stages are RC coupled. While leveling is not necessary to attain the required frequency response, the distortion of the amplifier was found to increase very rapidly with overdrive. An automatic level control was added and ensures very low distortion levels for a $\pm$3 dB range of input drive levels. The unusually high efficiency of this design is basically due to the transformer coupling of the output stage and to careful design of the circuits for excellent output matching without internal power-consuming terminations.

4.2.2 Output Stage

The most difficult part of the power amplifier is the output stage. The combination of wide bandwidth and low distortion requires transistors capable of high current and very high bandwidth. There are not many types available and economy dictates best use of the power capabilities; about 1-1/2 watts of RF output is required from the output transistors. It was decided to use a pair of NEC V773T transistors. They are in a strip-line package with an insulated stud and are rated at 5 watt dissipation with 75°C stud temperature. It would have been possible to use the two transistors in

parallel and get favorable matching conditions at the output, but the push-pull transformer-coupled configuration was chosen for its lower even-order harmonics and best use of the voltage and current capabilities of the transistors. The output transformer is a 200Ω-balanced-to-50Ω-unbalanced transmission-line variety. Early units were made here but a commercial product (Z-Match, Model HF 122) was found to be satisfactory. The output required is about 7V rms. At the secondary of the transformer, almost 10V rms are required because of series isolation resistor, detector loading and other losses. The primary voltage is about 20V rms. An 18V DC supply was found adequate but about 3V more are used to stabilize the operating point; the power supply requirements were established as -22V. The transistors are biased for lowest distortion at the required power level. Each transistor has a dc current of 140 mA, and 19V between collector and emitter, for a dissipation of about 2.7W, well within the rated 5W at 75°C stud temperature.

The output transistors are driven from a transmission-line transformer 50Ω-unbalanced-to-50Ω-balanced. The transformer is either an Anzac TP101 or Z-Match HF110. The output matching takes advantage of the characteristics of the transformer and frequency-dependent negative feedback and little power is wasted in internal resistive terminations.

4.2.3 Driver Stage

A single-ended class A amplifier in grounded-emitter configuration provides drive for the output stage. Negative feedback shapes frequency response and impedances. The transistor is a NEC 2SC1251 strip-line package with insulated stud. The dissipation in this stage is about 0.9W; the transistor is rated 2W at 75°C stud temperature.

4.2.4 Input Stage

This stage uses a 2N5109 in a class A, grounded-emitter

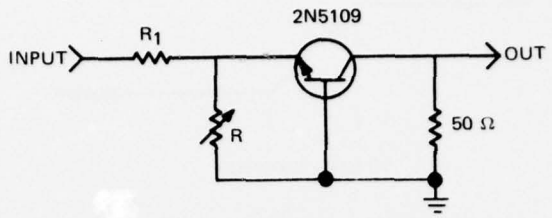


Figure 4.2.5. Gain Control Stage.

amplifier configuration. Negative feedback is used to shape frequency response and impedances. The dissipation is about 0.35 watt. A small radiator such as Thermalloy 2226 will hold the case temperature to less than 75°C (at max specified ambient); the transistor is rated 2.5W under these conditions.

4.2.5 Gain-Control Stage

Gain control over a modest range (±3 dB) is provided by the basic arrangement shown in Figure 4.2.5. The grounded-base transistor is driven from the input thru R1 chosen to ensure good input matching. The variable resistor R changes the gain; a PIN diode provides electronically variable gain. A diode with long lifetime keeps distortion low at the lowest frequency (0.8 MHz). The transistor is a 2N5109 with about 0.3W dissipation. As the transistor is rated 0.7W at 75°C ambient, no radiator or sink is required.

4.2.6 Shaped Level Control (SLC)

An automatic-level-control circuit prevents departures from proper input level and resultant high distortion. As the output specifications call for +29 dBm minimum to 20 MHz and +24 dBm minimum above 20 MHz, the level control must be shaped. Figure 4.2.6.1 shows the response, and Figure 4.2.6.2 shows the response-shaped rf detector and the basic arrangement of the control loop. A portion of the rf output is rectified and the

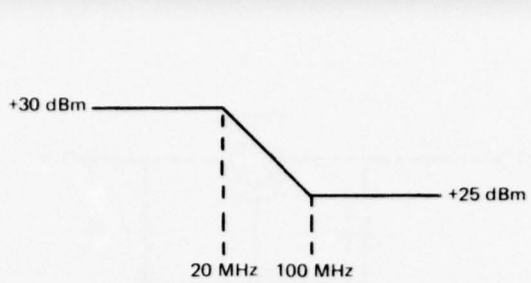


Figure 4.2.6.1. Response of Shaped Level Control.

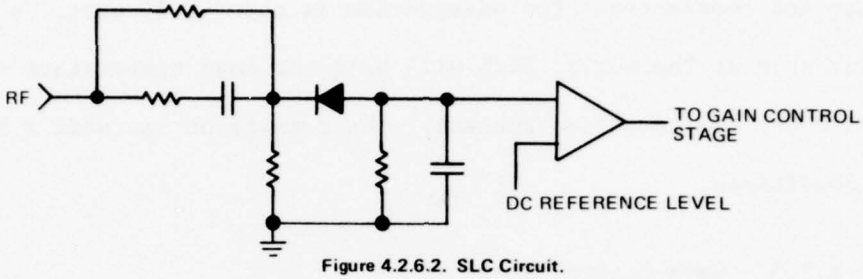


Figure 4.2.6.2. SLC Circuit.

dc from it is compared to a dc reference voltage. Any error between the two is used to vary the gain in the gain-control stage.

4.3 Reference IF and Phase Shifter

4.3.1 General

The 80-kHz signal from the Reference IF Mixer is fed to a phase-shifter which provides continuously adjustable phase over more than 360°. A dc signal is used to control the phase-shift; remote programming is possible.

The phase shifter is a phase-locked oscillator with a lock-loop that permits any phase relation between the reference signal and the oscillator output. Figure 4.3.1 shows the basic arrangement. The Reference IF Signal and the output from the voltage-controlled oscillator (VCO) are compared in the phase detector, which produces a dc output directly proportional to the phase difference between them. Zero output from the phase detector corresponds

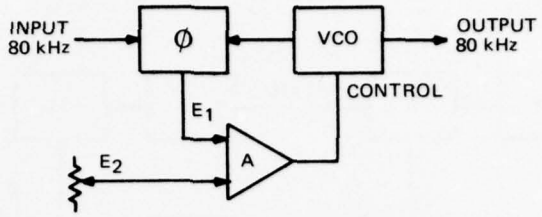


Figure 4.3.1. Basic Phase Shifter Circuit.

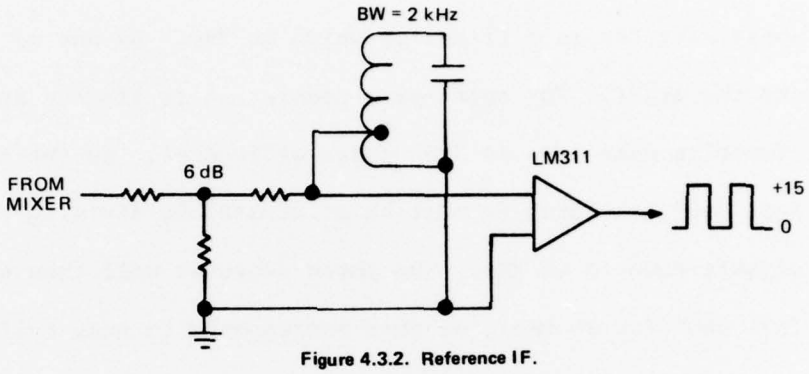


Figure 4.3.2. Reference IF.

to zero phase difference and maximum output corresponds to 360°. If the dc amplifier A has large gain, E_1 must equal E_2 and, as E_1 is proportional to the phase difference, so is E_2 the dc programming voltage. Very good linearity can be obtained and, if a potentiometer of adequate linearity is used, better than 1° accuracy is practical. This compares favorably with the 5° required.

4.3.2 Reference IF

The signal from the mixer is fed through a 6-dB attenuator (to provide mixer termination) to a single tuned circuit that defines the bandwidth. A digital comparator provides a square-wave signal of nearly B+ amplitude to drive the digital circuitry of the phase shifter. Figure 4.3.2 shows the circuit.

4.3.3 Phase-Shifter

The basic circuit as shown in Figure 4.3.1 has several limitations.

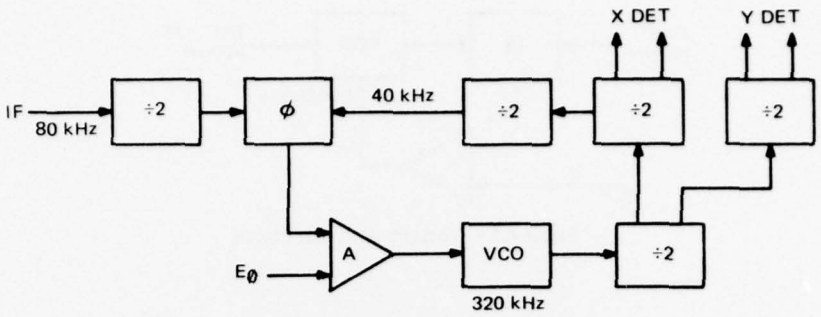


Figure 4.3.3.1. Phase Shifter.

First, the phase-detector is a flip-flop which is "set" by one of the signals and "reset" by the other. The pulse-pair resolution is limited and as a result it does not function near zero or 360° phase difference. As the specifications call for a full 360°, the problem must be eliminated by dividing both of the 80-kHz signals down to 40 kHz. The phase detector will then easily handle the full 360° (at 80 kHz), as this corresponds to only half the theoretical capability at 40 kHz. By proper choice of circuitry, the 0-360° phase difference at 80 kHz is made to correspond to 90° to 270° at the 40 kHz phase detector. This not only provides more than 360° capability but also improves the linearity of the programming.

As it was decided to use switching type synchronous detectors, four reference signals precisely 90° apart are needed at 80 kHz. By running the VCO in the lock-loop at 4 times 80 kHz, reference signals for the synchronous detectors can be generated with digital accuracy. The arrangement of the phase-shifter circuitry is shown in Figure 4.3.3.1. The VCO runs at 320 kHz. A series of flip-flops divides the signal and generates the drive signals for the X and Y detectors.

It was originally intended to use a crystal oscillator for the VCO but the several 320-kHz CT-cut crystals investigated did not provide enough voltage control (insufficient frequency pulling) without mode jumping. After considerable effort, an LC-oscillator was substituted. Frequency pulling

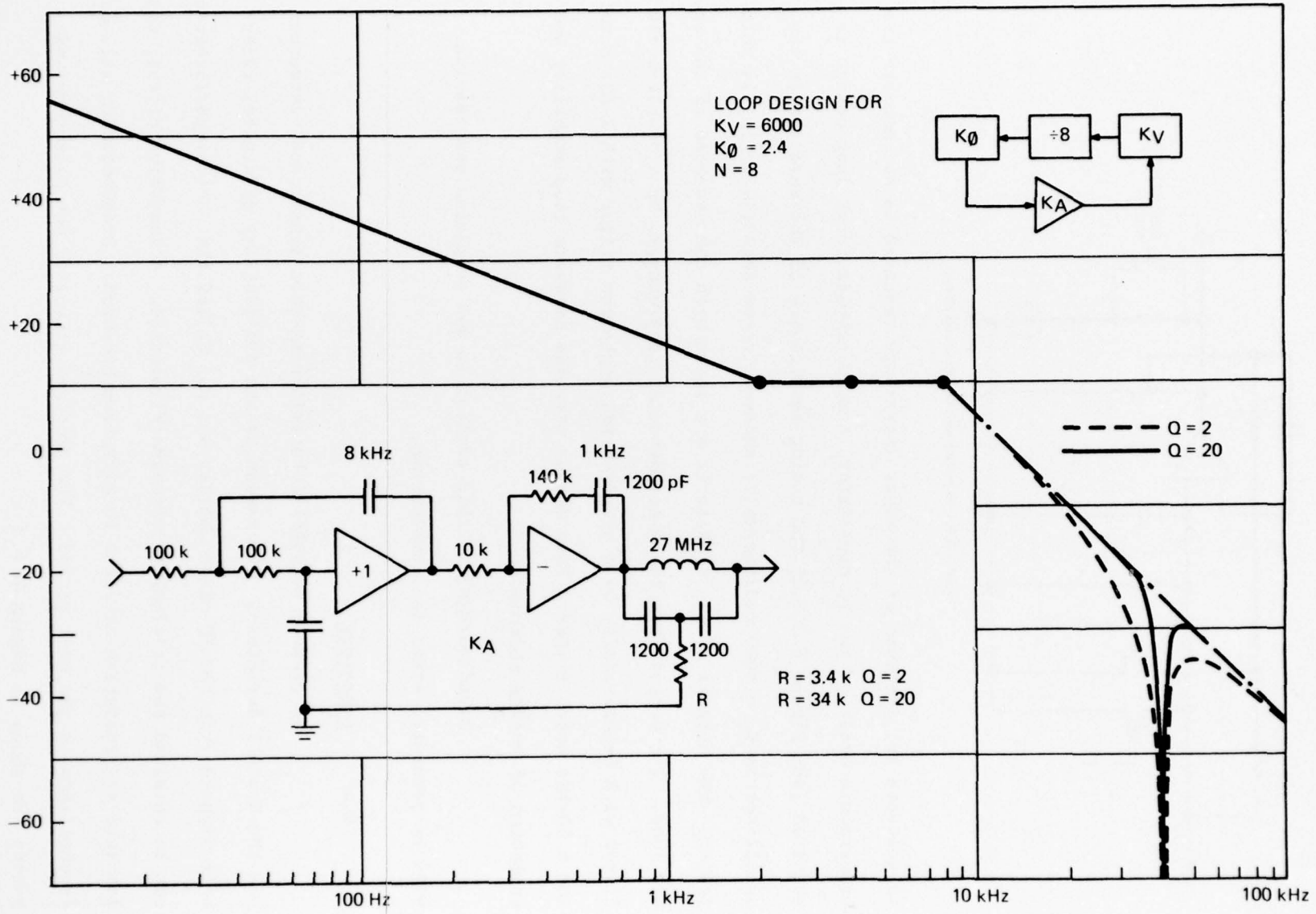


Figure 4.3.3.2 Circuit Diagram and Response of VCO Loop

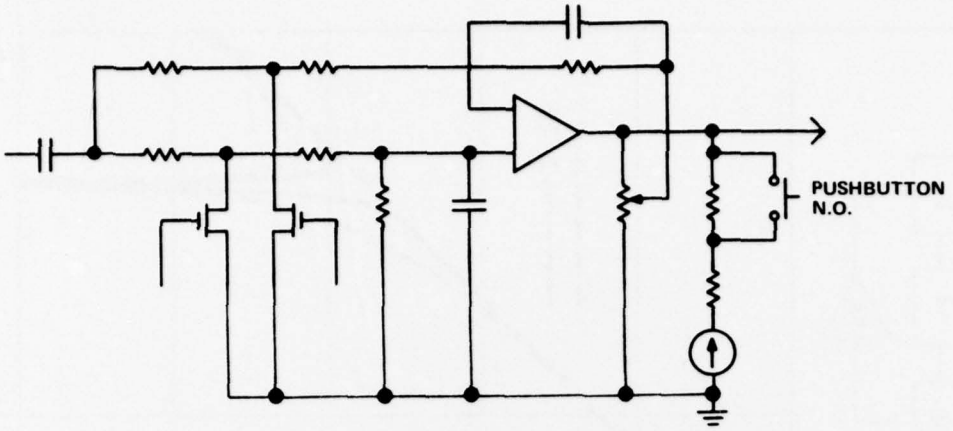


Figure 4.4.1. Synchronous Detector and Meter.

is adequate but, because of the wider lock-range required to accommodate the temperature drift of the LC oscillator, a more complex servo loop design is required (see Figure 4.3.3.2).The tuning sensitivity of the varactor in the oscillator is K_V = 6000 rad/sec/volt; phase-detector sensitivity is 2.4 volt/radian. The details of the K_A circuit are shown with the response of the overall loop. The output from the phase detector is processed by a double-break filter with 8-kHz cutoff, by a single-break high-pass filter with 2-kHz cutoff, and a 40-kHz notch filter. This design provides adequate loop stability and rejection of 40-kHz sidebands.

Breadboarding of this section is not completed and results will be presented after full evaluation.

4.4 Detectors

We propose to substitute switching-type synchronous detectors for the X and Y detectors. The reason is the availability of digital reference signals from the IF phase shifter and our belief that better performance can be obtained and critical adjustments eliminated. A tentative circuit was designed and resistive networks in microform procured. Breadboarding will be accomplished in the next period. The proposed circuitry for detectors and meters are shown in Figure 4.4.1 .

4.5 Power Supplies

Power-supply requirements have been established. The rf module has a totally separate power-supply system (as required by the specifications) with two voltages: -22 V at about 0.6 A regulated and -5.2 V at about 0.4 A. The -5.2 V is used for the digital circuitry (ECL) and the -22 V for all others. Most of the -22 V power goes into the Broadband Power Amplifier.

All other sections share a second power-supply system which provides $\pm$15 V regulated. Total power requirements have not been established at this time.

The two power transformers with their rectifiers and filters will be located on the main frame of the instrument. The location of the regulators has not yet been decided. Some cards may have individual on-board regulators if little enough power is dissipated so that no heat-sinking is required.

Section 5

CONCLUSIONS

5.0 Conclusions

5.1 X10 Frequency Multiplier

A complete X10 Frequency Multiplier unit, using the design techniques described herein, has been breadboarded and evaluated. The unit operates satisfactorily in all respects and in compliance with specifications. Work is under way on the design of the etched circuit layout, which will consist of a single 2-1/2 x 8-inch board housed in an RF shield compartment. Parts lists and drawings have been made, a test fixture and power supply assembled, and prototype parts have been ordered. The initial design phase of this effort is therefore concluded. Further work now awaits etched-board fabrication.

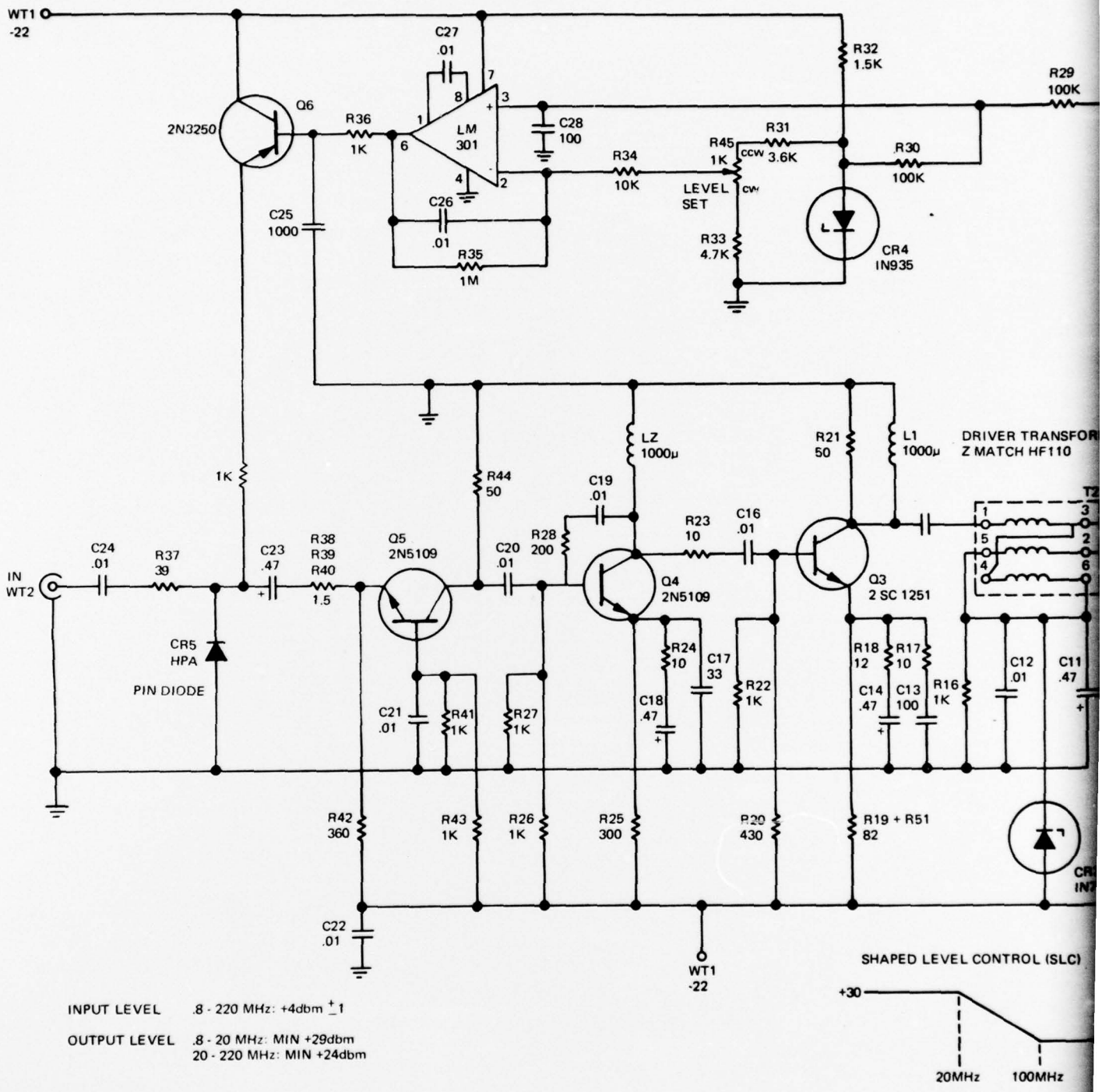
5.2 Broadband Power Amplifier

No commercially available power amplifier was found that met the requirements of this application. So a design effort was undertaken which has produced a special-purpose wideband power amplifier with the necessary performance characteristics.

The breadboard unit was constructed in an aluminum housing 5 x 2-1/2 x 1 inches. Total dc input power is less than 10 watts. The measured performance of the amplifier is satisfactory except that, at the high-frequency end, the output match is not in specification. As the deviation is caused entirely by the series inductance of the output lead, it is expected that proper layout on an etched-circuit card will eliminate this problem; other corrective means are available, if needed.

Figure 5.2.1 shows the schematic amplifier breadboard. The final etched-circuit version will require some changes, mostly in the response-shaping components. The use of a negative power supply permits the most favorable arrangement of the output stage without causing any difficulties elsewhere. The transmission-line transformers are standard commercial products.

The frequency response and distortion of the amplifier are shown in Figure 5.2.2. The return loss at the output is shown in Figure 5.2.3 and the output impedance is also shown in Smith Chart format in Figure 5.2.4. Note that the specification are not met over 190 MHz. The Smith Chart confirms that this is caused by series inductance which will be eliminated on the etched-circuit version. If the inductance cannot be reduced, a small compensating capacitor (from output terminal to ground) will bring the VSWR into specs at high frequencies.


WT1
-22
C27
.01
R32
1.5K
R29
100K
Q6
2N3250
R36
1K
LM
301
C28
100
R31
3.6K
R45
1K
ccw
R30
100K
R34
10K
LEVEL
SET
cw
C26
.01
C25
1000
R33
4.7K
CR4
IN935
R35
1M
LZ
1000µ
R21
50
L1
1000µ
DRIVER TRANSFOR
Z MATCH HF110
1K
R44
50
C19
.01
C24
.01
R37
39
C23
.47
R38
R39
R40
1.5
Q5
2N5109
C20
.01
R28
200
R23
10
C16
.01
IN
WT2
Q4
2N5109
Q3
2 SC 1251
CR5
HPA
PIN DIODE
R24
10
C17
33
R18
12
R17
10
C12
.01
C11
.47
C21
.01
R41
1K
R27
1K
C18
.47
R22
1K
C14
.47
C13
100
R16
1K
R42
360
R43
1K
R26
1K
R25
300
R20
430
R19 + R51
82
C22
.01
WT1
-22
SHAPED LEVEL CONTROL (SLC)
+30
20MHz
100MHz
INPUT LEVEL .8 - 220 MHz: +4dbm ±1
OUTPUT LEVEL .8 - 20 MHz: MIN +29dbm
20 - 220 MHz: MIN +24dbm

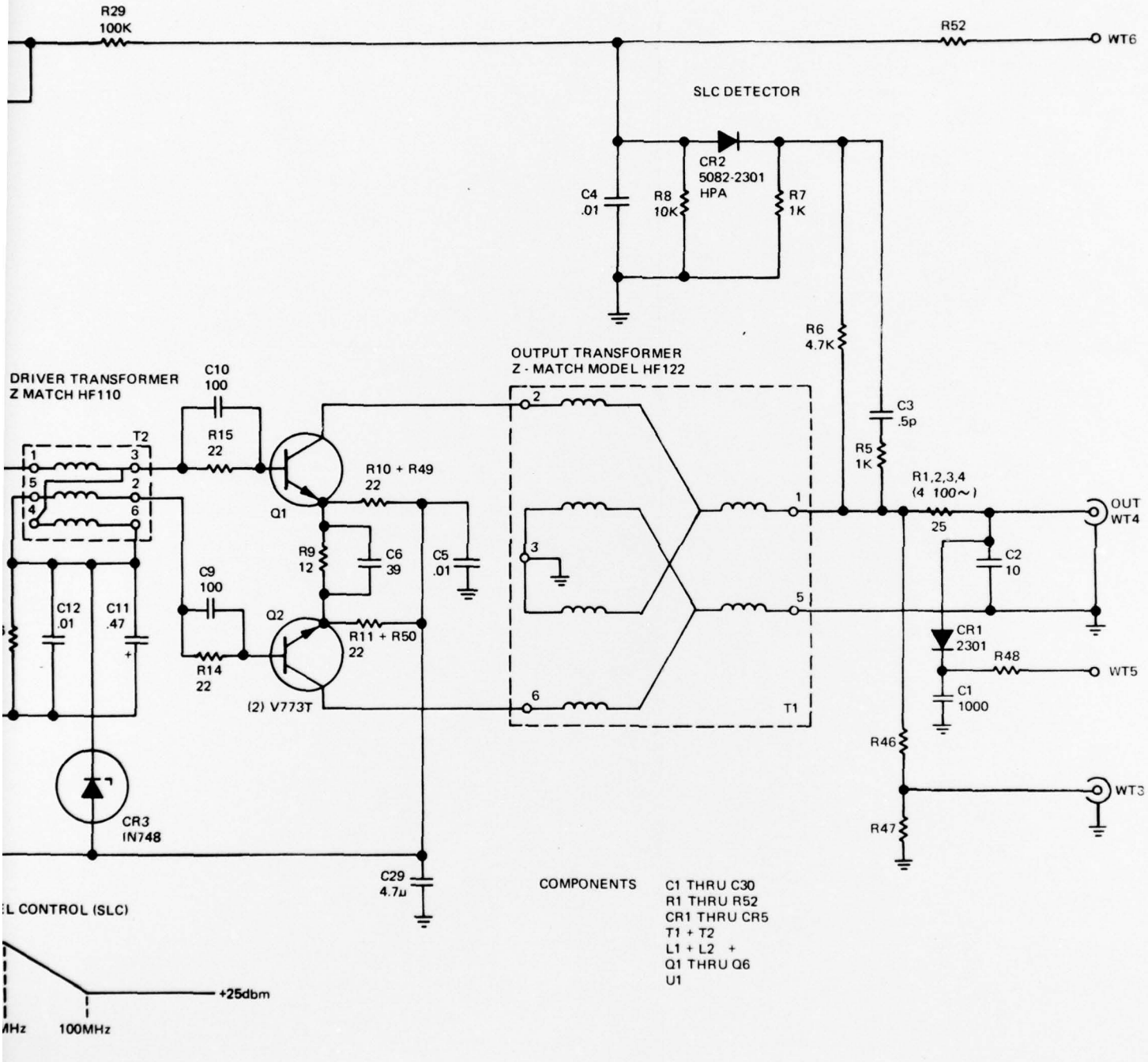


Figure 5.2.1 Circuit Diagram of RF Power Amplifier

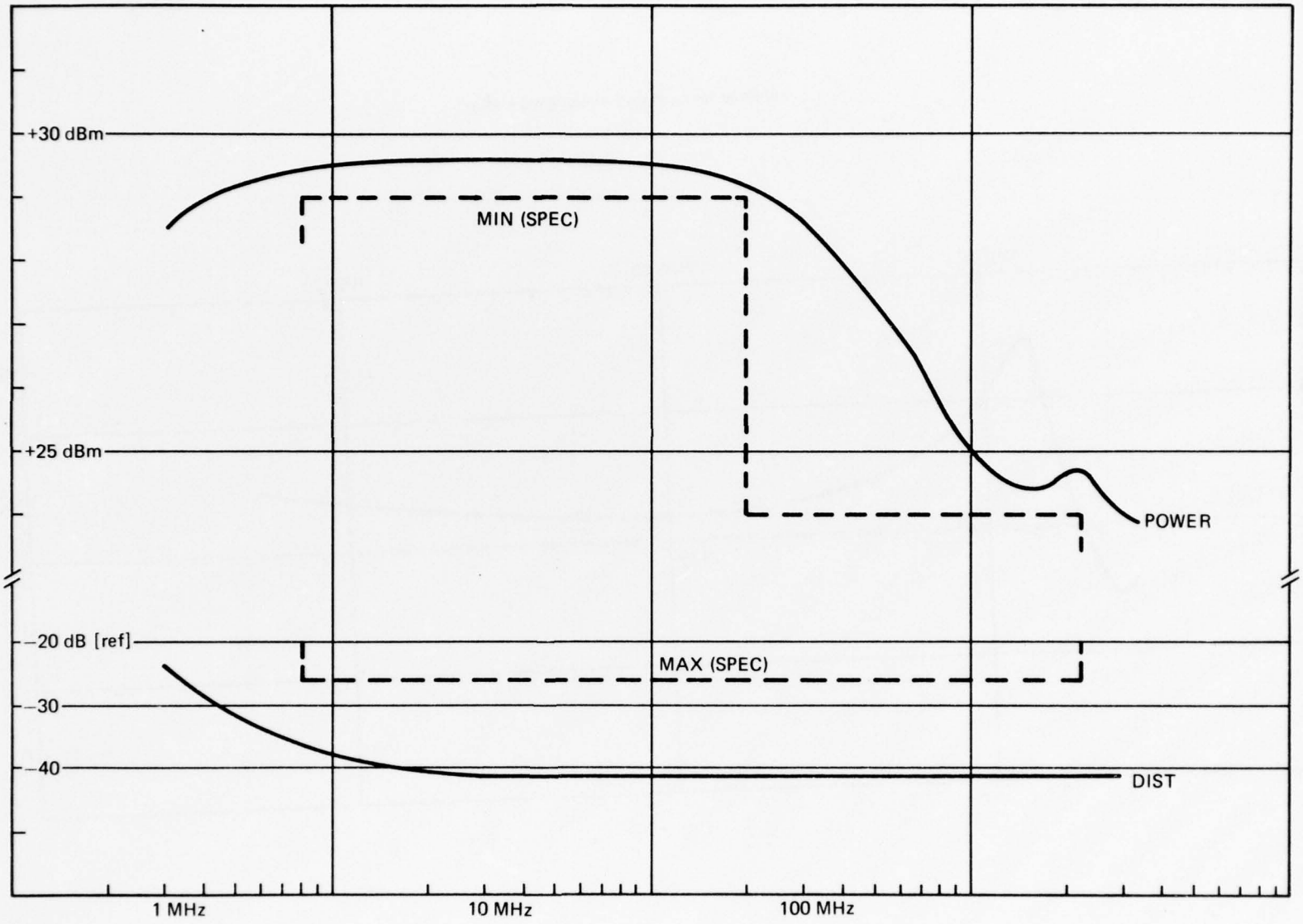


Figure 5.2.2 Frequency Response and Distortion of Power Amplifier

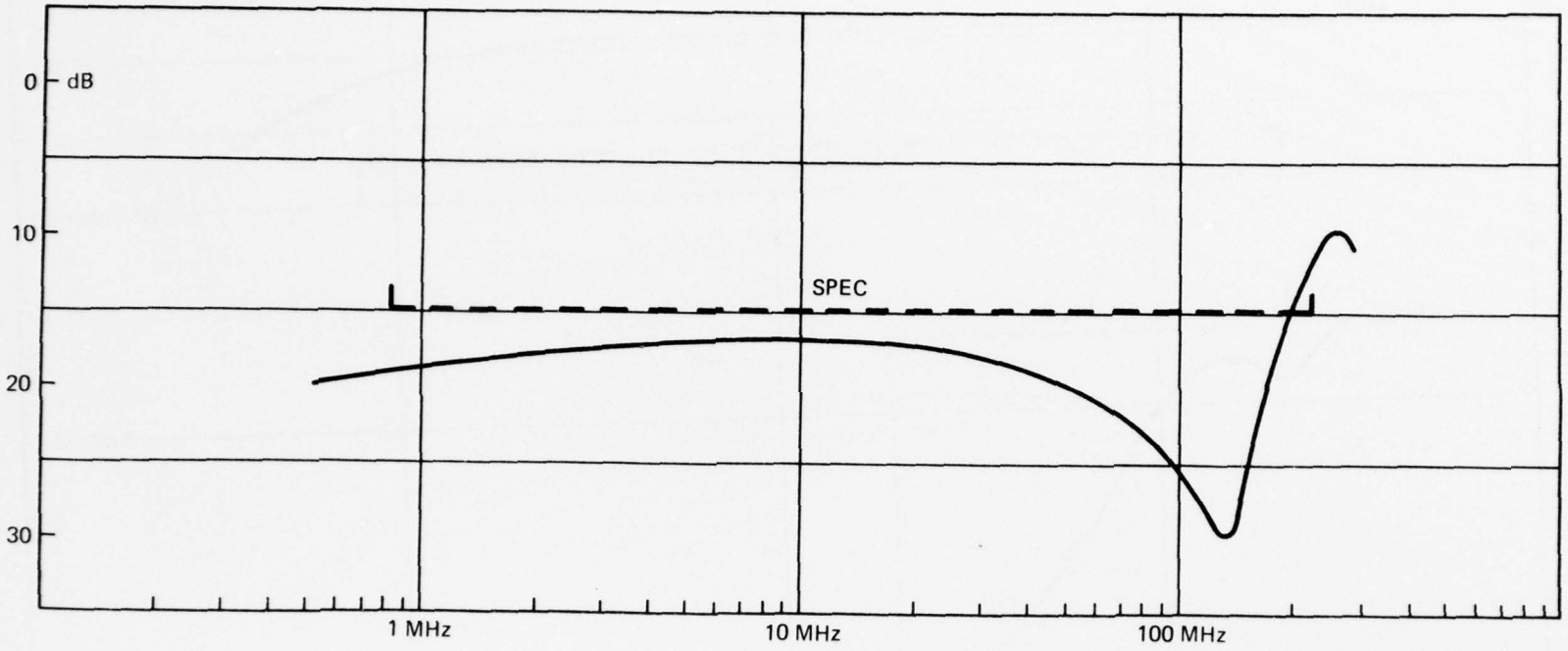


Figure 5.2.3 Return Loss of Power Amplifier

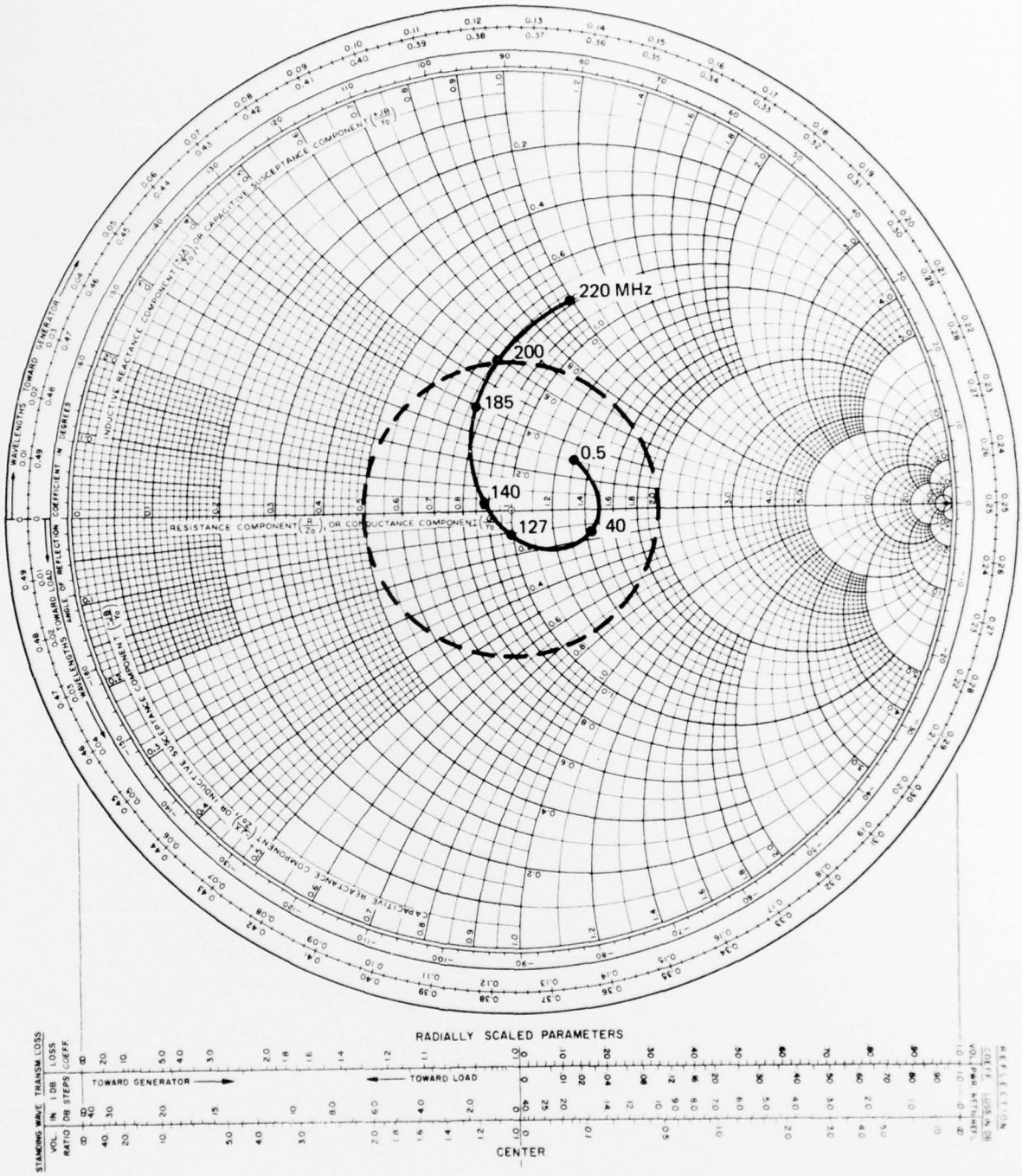


Figure 5.2.4 Smith Chart Impedance Plot – Power Amplifier Output

Section 6

6.0 Program for Next Interval

Most of the breadboarding will be completed during the next period as well as initial phases of mechanical design, panel layout and extensive electrical evaluation of complete etched circuit cards. Particular effort will be required for the IF amplifier. Reference IF phase-shifter and synchronous detectors.

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This report summarizes the work done to date on the X10 Frequency Multiplier and Broadband Power Amplifier sections of the Tracking Servobridge Detector. Preliminary design decisions and general concepts for other component system sections are also described.

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